

ABSTRACT

A packaging assembly for semiconductor devices and a method for making such packaging is described. The invention provides a non-Pb bump design during a new flip-chip method of packaging. The design uses special conductive materials in a stud form, rather than a solder ball containing Pb. This configuration maintains a desirable solder thickness between the die and the leadframe and forms a high standoff by restricting solder wettability on the leadframe side. This configuration also absorbs any stress and protects the die from cracking. The invention also provides methods for making such semiconductor packages.